Distributed clock generator for synchronous SoC using ADPLL network

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***Abstract*— In this paper a novel architecture of on-chip clock generation employs a network of oscillators synchronized by a network of all-digital PLLs (ADPLLs). In the implemented prototype 16 local clock generators are synchronized by the ADPLL network, with an output frequency of 1.1-2.4 GHz. The synchronization error between the neighboring clock domains is less than 60 ps. The fully digital architecture of the generation offers flexibility and efficient synchronization control suitable for use in synchronous SoCs.**

I. Introduction

Clock generation and distribution are one of the main challenges in the design of modern large scale SoC [1]. The increase of relative dimensions of digital SoCs, together with power limitations, makes the techniques of centralized clocking prohibitive. While long transmission lines are needed for chip-wise clock distribution, the associated delays must be perfectly mastered. This is very difficult to obtain without unacceptable power consumption costs. This is the main reason for the popularity of globally asynchronous SoC architectures, which however present a number of fundamental drawbacks related with reliability and verification issues, as well as suffering from reduced communication speed.

Distributed clock generators are based on the local oscillators distributed over the chip area, mutually coupled with its immediate neighbors so that all oscillators have the same phase and loaded with the local clock tree. The network of oscillators is sufficiently dense, so that: (i) geometric distance between each couple of neighboring oscillators is small enough for delays associated with the network oscillator links to be negligible, (ii) distribution of the clock signal inside of each clocking domain is done by conventional techniques without difficulties and (iii) synchronous communications between neighboring zones is possible as far as the corresponding local oscillators are synchronous in phase. Here, long clock distribution lines employed by conventional architectures are replaced by local short network links which connect small local clock trees. When local oscillators are coupled in the phase domain, the system is called Distributed PLL Network. The latter is a good candidate for on-chip distributed clock generation, because of better compatibility with digital circuits.

This paper presents a first digital implementation of an array of 16 oscillators coupled through a network of all-digital phase locked loops (ADPLLs) intended for distributed clock generation. The proof-of-concept chip generating 1-2.5 GHz clock is implemented in 65 nm CMOS technology.

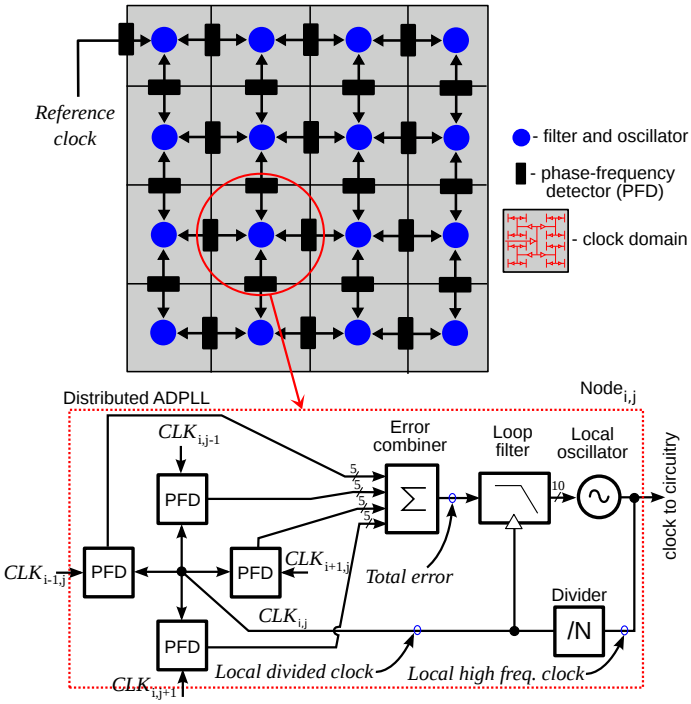

Fig. 1. Architecture of the ADPLL network and of a single node.

The theoretical basis for this system was provided by the studies [2], [3], [4], while the only silicon implementation of this concept employed a network of analog PLLs [5].

II. Distributed clocking architecture

A. System description

The structure of the clocking network is presented in Fig. 1. The local clocks are generated by digitally controlled oscillators (DCOs). 24 digital Phase-Frequency Detectors (PFD) measure the timing error between each couple of neighboring DCOs. The network is coupled with the external reference clock through a PFD placed in upper left corner of the network. The digital error signals from PFDs are processed by the digital proportional-integral (PI) loop filters. Each filter processes the weighted sum of the errors from up to 4 PFDs (depends on topological position of the node) and generates the digital control code for the DCO. The control objective of the filter is to maintain the sum of the errors close to zero. Such

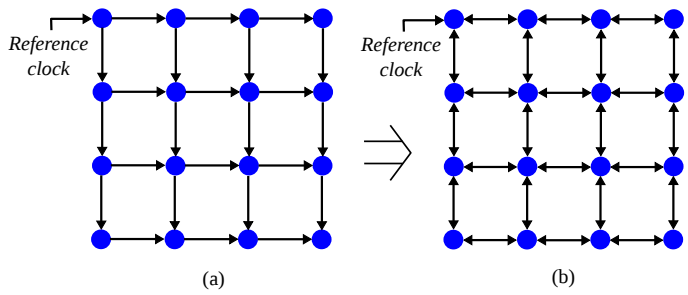

Fig. 2. Mode-lock elimination technique: (a) power up in unidirectional configuration and after convergence swithcing to (b) bidirectional configuration.

a network, if properly designed, synchronizes at the phase of the reference clock.

B. Stability issues

The paramount question about the stability of such a complex dynamical system was addressed in theoretical studies through control theory tools [3], [4]. A formal proof of stability, together with an algorithm of choice of the block parameter was proposed. In addition to this, several studies of PLL networks highlight the existence of multiple synchronized modes in which all oscillators have the same frequency and a fixed (zero or not) phase errors. Only the mode with a zero phase error is required for the clocking application. The selection of the desirable synchronized mode is particularly easy in digital PLL network because of its ability of reconfiguration.

C. Desirable mode selection

The proposed method is based on an on-fly dynamic reconfiguration of the network [8]. The reconfiguration procedure is performed during the start-up and consists of two steps:

Step 1. The clocking network is powered up and programmed into a unidirectional configuration. This is achieved by programming the feedback links between nodes; by disabling or enabling them. For example, each node receives the information about errors from upper and left neighbors Fig. 2(a). In such a mode information about reference frequency and phase propagates from the left upper node to the lowest right corner of the network. This mode excludes the cycles of propagation of information, hence eliminates the possibility of undesired locking. However, in such an operation mode the suppression of perturbations is weak [8] and clocking network has the accumulative errors. They increase with the distance from the reference point and introduce an undesired skew.

Step 2. Once the network is synchronized with certain timing errors, it is programmed into a bidirectional configuration Fig. 2(b). In this mode the reverse links are activated, and the network operates in a fully synchronous mode with distributed feedback (coupling) maintaining the synchronization.

Thus, when the required synchronization mode is selected, the timing errors between neighboring local clocks are close to zero.

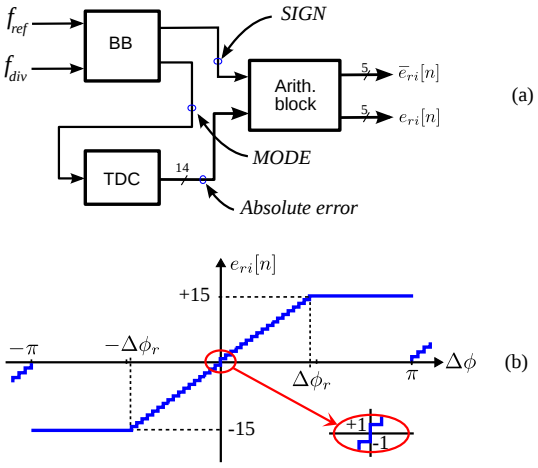

Fig. 3. PFD: (a) block diagram and (b) its transfer function.

III. Node Architecture

A. Phase-frequency detector overview

The PFD is an analog-to-digital converter quantifying the synchronization error into a digital 5-bit signed number. According to its transfer function, Fig. 3(b), its range is limited by the boundaries $\pm\Delta\phi_r$, which are derived from the constraints of precision and hardware complexity. The detail block diagram of the PFD is shown in Fig. 3(a). The PFD consists of a bang-bang phase detector (BB) measuring the sign of the phase error and a time-to-digital converter (TDC) for the quantification of the absolute time error between two clocks. The arithmetic block combines the signals from these blocks and produces two binary signed signals (straight and inverted) thereafter used by the local and neighboring nodes.

The bang-bang detector is a state automaton which decides which of two input rising edges of clock signals arrived first. The use of an arbiter circuit and metastability filter in this circuit makes it robust to metastability effects [7].

The TDC is based on a tapped delay line followed by the sampling register. The delay elements are CMOS buffers with delay 32 ps.

B. Digitally controlled oscillators

The implemented DCOs are the ring CMOS oscillators employing width-modulated technique for the digital frequency tuning [6], [7]. Their structure is based on a 7-stage ring oscillator (Fig. 4) with a parallel connection of the tuning inverters (Fig. 4, CTI0-CTI6 and FTI0-FTI2) in each stage of oscillator. The main inverters (Fig. 4, MI0-MI6) are always active and define the lowest oscillation frequency. The tuning inverters distributed over all 7 stages of oscillator and divided on two arrays: 256 coarse tuning (CTI) and 3 fine tuning (FTI) inverters. They provide respectively 6 MHz and 1.5 MHz frequency tuning steps with a total of 256×4=1024 steps. The cells are controlled by three thermometer codes obtained from the binary to thermometer decoders. The monotonicity of the code-frequency characteristic is guaranteed by an appropriate

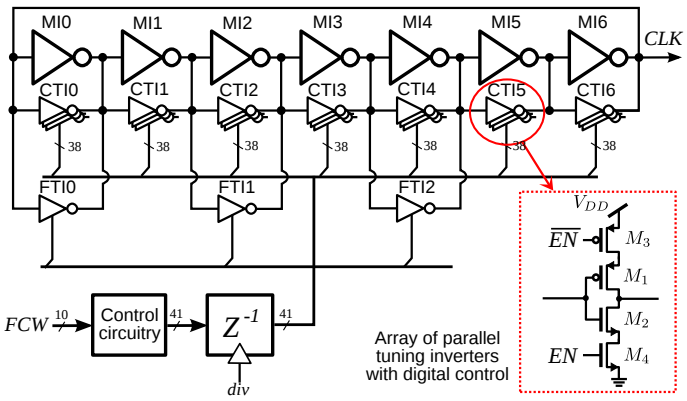

Fig. 4. Digitally controlled oscillator based on a 7 stage CMOS ring oscillator.

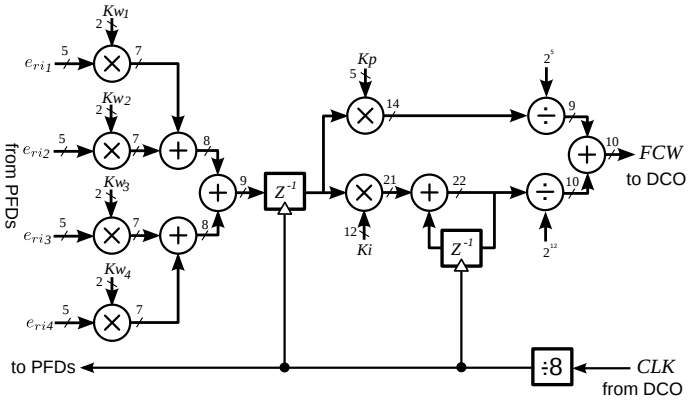

Fig. 5. The error combiner and proportional-integral filter.

choice of the control algorithm. The designed in 65 nm technology oscillator has a frequency tuning range 1-2.5 GHz.

C. Error processing

The error processing in node is performed in two steps by an error combining block and a loop filter.

The first block receives up to four 5-bit 2-complement coded errors. They are passed through four variable gain blocks and then summed using four-input adder. The weighting coefficients of the variable gain $Kw_1 - Kw_4$ are programmable. Each gain can take independently a value from the set {0,1,2,4} and implemented as a binary shift, so introducing a very small delay. Programming these coefficients, we can control the connectivity between the nodes of the network. Then the four-input adder operates with 7-bit operands and produces a 9-bit sum. The output of the adder is buffered with a register. We mention that each node is an auto-sampled system: the filter is sampled with the generated local clock divided by 8 and PFDs compare the clocks at this rate.

The PI filter processes the 9-bit sum of the errors. It has coefficients K_p and K_i programmable with respectively 5 and 12-bit resolution.

Both blocks have been designed in a common digital design flow with a use of standard cells.

IV. Test circuit design

A prototype of the distributed clock generator with 16 nodes has been designed and manufactured in 65 nm CMOS technology. It has an area of ≈2 mm^2 where the clock network itself occupies 0.8×0.9 mm^2 (Fig. 6). Besides the clocking network, the on-chip digital circuitry includes design-for-test block, the PFD and bang-bang detector for their characterization. The microphotograph of the fabricated silicon prototype is presented in Fig. 6.

V. Measurement results

The goal of the experiments were the characterization of the phase synchronization between the DCOs and an investigation of the sensitivity of the network to different perturbations.

The measured initial frequencies of the oscillators are distributed within a 47 MHz range, which gives good conditions for the fast start-up of the network. This range is explained mainly by the sensitivity of the oscillators to the supply voltage, which is measured to be ≈900 MHz/V. However, even with this result, the desired frequency adjusting range and convergence of the network are assured under ±10 % supply variation. The achieved average nominal frequency in the clocking domains is 1744 MHz, while the tuning range is 1100-2380 MHz.

Fig. 7 presents the captured waveforms of divided by 16 local clocks when the network is synchronized. The observed timing errors between neighboring clocks were in the range of 30-60 ps for 1.6 GHz output frequency. This is less than 10% of the clock period. This result can be improved by increasing the PFD resolution. As predicted by theory, the error is a zero-centered random process, i.e. the skew is zero.

An important result is that for 500 cases of network start-ups we haven't observed the undesired locking states. This result is in a contradiction with modeling and the theory: the possibility

Fig. 6. Die microphotograph.

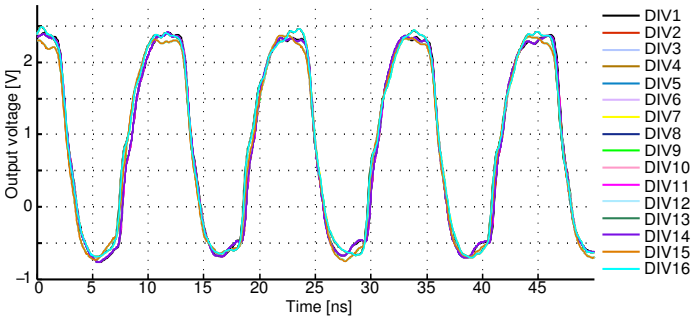

Fig. 7. Captured phase locked divided clocks.

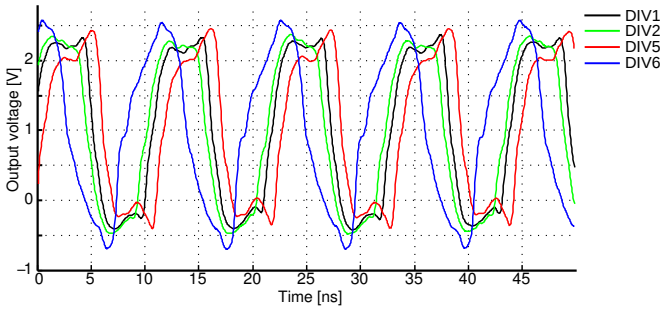

Fig. 8. Captured divided clocks in mode-lock state.

of mode-locking is one of particular properties of the PLL networks which is always mentioned in theoretical studies [2] and reproduced in prototype [9]. Therefore, the research of mode-lock states was repeated with reduced 2×2 network configuration, where theoretically mode-lock must occur with high probability. In such a configuration, for 500 attempts of perturbation by global reset we have observed a mode-lock 4 times. One of these states has been captured and it is shown in Fig. 8.

Fig. 9 shows the transient process in the one of the oscillators. The perturbation has been introduced in a network in order to study the robustness of the network at t =8 μs. After this perturbation, the clocking network returns to the reference frequency and phase after 17 μs. The frequency acquisition speed may be increased by employing special techniques more efficient than a simple PI filtering.

In order to check the robustness of the network operation in presence of variation of the block parameters, several experiments were done. In particular, the network was tested under 10% variation of the filter coefficients: no degradation in the quality of the oscillator synchronizaton was observed.

The power consumption of the clocking network has been measured for 1.6 GHz oscillation frequency under 1.2 V supply voltage. The PFDs and PI filters consume 32 mW (≈2 mW per node). The DCO consumption is 9.8 mA/node (≈6.15 mW/GHz). We note that the power optimization of the DCO was not an objective of this prototype and better results can be obtained by a more involved design.

Table I shows a performance summary of the measured results and comparison with existing implementation of the distributed clock generator.

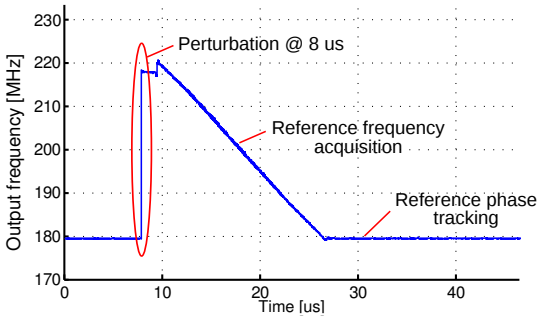

Fig. 9. Transitional process in Node 11.

TABLE I
NETWORK TEST CHIP MEASUREMENTS SUMMARY AND COMPARISON

Parameter	**[5]**	***This work***
Number of nodes	16	16
Central frequency of the SCA, MHz	1200	1744
Frequency range, MHz	1100∼1300	1100∼2380
Timing error, ps	30	$<$ 60*
Power consumption, mW	390**	186.2***
Technology, nm	350	65
Clocking core area, mm^2	-	≈0.72
Chip area, mm^2	≈9	≈2.04
Circuitry nature	analog	digital

* between neighbor nodes
** F_{clk} = 1.2 GHz
*** mixed and digital @ F_{clk} = 1.6 GHz

VI. Conclusion

A distributed clock generator for synchronous SoC based on the network of coupled in phase oscillators has been demonstrated. The synchronization of the oscillators is achieved by the ADPLL network. The problem of undesirable synchronization modes is solved by a dynamic reconfiguration of the network interconnection topology at the start-up stage. The advantage of the proposed system is compatibility with the digital environment, its flexibility of reconfiguration and possibility of advanced control over the clock generation. The fabricated prototype has proved the reliability of the proposed clock generation methodology. It has 16 nodes and operates in a frequency range 1.1-2.4 GHz. The measured timing accuracy between neighboring clocking domains of the circuit is less than 60 ps.

Acknowledgments

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